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EXAMINER	
ROBERTS, JESSICA M	

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2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,897	CHEEDELA ET AL.	
	Examiner	Art Unit	
	JESSICA ROBERTS	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/03/2010 has been entered.

Response to Arguments

2. Applicant's arguments filed 05/03/2010 have been fully considered but they are not persuasive.

As to Applicants argument regarding the Holmes decision. The examiner respectfully disagrees. It was decided that in this case, the invention involved more than merely separating task into separate task. The differences between the claimed invention and the Gammage et al. lie in not merely the separating of an internal message path selection task into separate task, but rather the use of an external path selection feature to perform message path selection external to and independently of the message sending and receiving objects, which as stated by the BPA, involved more than just a separation of parts. Thus, the Holmes case is not applicable in this case.

As to Applicants argument regarding the Parnell decision. The Examiner respectfully disagrees. The Pennell decision was based on 102 and 103, where the

examiner failed to provide a basis in fact and/or technical reasoning to support alleged inherent characteristics necessarily flows for the teaching of the prior art. The rejection is not based on inherency, further there is rational to support the legal conclusion of obviousness in the rejection. Thus, the Pennell rejection is not applicable.

As to Applicants argument regarding the Gruden decision. The Examiner respectfully disagrees. The Gruden decision was based on hindsight based on the appellants own teachings to provide reason for one of ordinary skill in the art to consider a modification to arrive at the claimed invention, which is not applicable in this case.

As to Applicants argument that AAPA does not teach a register for storing a portion of the reference pixels...".

The Examiner respectfully disagrees. AAPA discloses where during decoding, the motion vectors are used to retrieve the reference pixels. The reference pixels are retrieved from a memory storing the reference frame. The memory storing the reference frame is known as a frame buffer. A motion vector address computer determines the appropriate addresses storing the reference pixels for a macroblock, based on motion vectors, [0007], which reads on the claimed limitation. Further, the frame buffer as described by AAPA performs the same function as the claimed register. Thus, the examiner maintains that the AAPA reads upon the claimed limitation.

Status of Claims

1. Claims 1, 2 and 4-12 are presently pending and claim 3 has been **cancelled** and claims 11-12 have been added by applicant's submission on 05/03/2010.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

   1. Determining the scope and contents of the prior art.
   2. Ascertaining the differences between the prior art and the claims at issue.
   3. Resolving the level of ordinary skill in the pertinent art.
   4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fimoff et al., US-6, 510,178 in view of Yuan et al., US-2005/0094729 A1 and further in view of Applicants Admitted Prior Art (AAPA).

6. Regarding claim 1, Fimoff teaches a decoder for decoding macroblocks, said video decoder comprising: a processor (fig. 5, decoder 100) for decoding a set of parameters, said set of parameters comprising motion vectors indicating reference pixels associated with the macroblock (abstract); a motion vector address computer for calculating addresses associated with motion vectors (column 29 line 34-49); a pixel reconstructor for reconstructing pixels from the macroblocks, the pixel reconstructor operable to reconstruct pixels from macroblocks encoded in accordance with a plurality of standards (column 6 line 50-58); said pixel reconstructor further comprising: a

macroblock input buffer for storing the reference pixels that are fetched from the frame buffer by the video request manager at the addresses calculated by the motion vector address computer (Fimoff teaches a method of reconstructing pixel blocks from P and B DCT coded blocks comprises the following steps: a) selecting reference pixel from a memory in response to a motion vector, column 6 line 50-55. Further, a motion vector translator 150 translates the received full resolution motion vector into a low resolution motion vector as previously described. The low resolution motion vector is then converted into reference picture memory addresses for supply to the memory 106, column 29 line 36-41. The reference pixels read from the memory 106 by the addresses from the motion vector translator 150 are supplied to a horizontal prediction filter, column 29 line 44-46. Therefore, it is clear to the examiner that Fimoff teaches a buffer to store the reference pixels that are addressed by the motion vector address computer, which reads upon the claimed limitation).

Fimoff does not explicitly teach a frame buffer for storing past and future reference pictures; a video request manager for fetching a block of reference pixels at the addresses calculated by the motion vector address computer; the reference pixels are fetched from the frame buffer and a register for storing a portion of the reference pixels that are fetched from the frame buffer by the video request manager at the addresses calculated by the motion vector address computer; and wherein the register, macroblock, input buffer, and frame buffers are separate, a frame buffer for storing past and future reference pictures,

However Yuan teaches a frame buffer for storing past reference pictures_(fig. 8); a processor-based system for encoding and decoding a plurality of standards for compression ([0037], [0108] and fig. 1, 4, 6, and 6). Yuan further teaches the reference pixels are located in frame buffer (fig. 8). The examiner notes that in order to retrieve the reference pixels from the frame buffer would necessitate the use of retrieve or call command or video request manager); the reference pixels are fetched from the frame buffer (fig. 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yuan with Fimoff for allowing for support video and audio application differing standards and formats without significant hardware overhead, Yuan [0037].

Fimoff (modified by Yuan) as a whole is silent in regards to a register for storing a portion of the reference pixels that are fetched from the frame buffer by the video request manager at the addresses from the frame buffer that were calculated by the motion vector address computer.

However, APPA a register for storing a portion of the reference pixels that are fetched from the frame buffer that are fetched from the frame buffer by the video request manager at the addresses from the frame buffer that were calculated by the motion vector address computer (During decoding, the motion vectors are used to retrieve the reference pixels. The reference pixels are retrieved from a memory storing the reference frame. The memory storing the reference frame is known as a frame

buffer. A motion vector address computer determines the appropriate addresses storing the reference pixels for a macroblock, based on motion vectors, [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Fimoff (modified by Yuan) with AAPA for providing efficient image processing.

Fimoff (modified by Yuan and AAPA) as a whole have the majority of the features of claim 1, but still fails to teach wherein the register, macroblock input buffer, and frame buffers are separate. However, it would have been an obvious modification readily apparent to one of ordinary skill in the art at the time of the invention since it entails to separate the register, macroblock input buffer, and frame buffers, which is merely to make separable, a distinction which the courts have already ruled against *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. of Int. 1969).

Regarding claim 2, Fimoff (modified by Yuan) as a whole teaches everything as claimed above, see claim 1. Fimoff is silent in regards to of Fimoff and Yuan as a whole further teach wherein the plurality of standards comprises MPEG-2 and AVC.

However, Yuan teaches wherein the plurality of standards comprises MPEG-2 and AVC (Yuan, Fig. 4, 6, and 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yuan with Fimoff for allowing for support video and audio application differing standards and formats without significant hardware overhead, Yuan [0037].

Regarding claim 4, Fimoff (modified by Yuan) as a whole teaches everything as claimed above, see claim 1. Fimoff is silent in regards to the wherein the pixel reconstructor (Fimoff and Yuan, decoder) comprises; a data path for outputting another portion of the reference pixels.

However, Yuan teaches wherein the pixel reconstructor (decoder) comprises; a data path for outputting another portion of the reference pixels (Yuan discloses the reference pixels are output to the motion compensation unit, fig.8, 800. The examiner notes that the frame buffer contains the reference frames, and reference frames are composed of reference pixels. Further, the reference frames are output to the motion compensation unit 812). More so, to output the reference pixels from the frame buffer, would necessitate the use of a data path.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yuan with Fimoff for allowing for support video and audio application differing standards and formats without significant hardware overhead, Yuan [0037].

Regarding claims 11 Fimoff (modified by Yuan and AAPA) as a whole teaches everything as claimed above, see claim 1. In addition, Fimoff teaches the video decoder of claim 1, wherein: during a first cycle the register stores reference pixels for a macroblock (Fimoff teaches a method of reconstructing pixel blocks from P and B DCT coded blocks comprises the following steps: a) selecting reference pixels from a memory in response to a motion vector; b)filtering the selected reference pixels to produce a filtered output; c) if the motion vector has 1/2 pixel resolution, adding a drift

compensation value to the filtered output; and, d) adding the filtered output to the P and B DCT coded blocks in order to form the reconstructed pixel blocks, col. 6 line 50-58. Thus, it is clear to the examiner that disclosed, is to select reference pixels that are stored in memory, and to apply a offset (adding a drift compensation value) to the reference pixels and forming the reconstructed pixel blocks, which reads upon the claimed limitation).

Fimoff does not explicitly disclose a register; a first half of a row of luma portion of a macroblock.

However, Fimoff discloses a memory (col. 6 line 50-58), and that in a decoder, it is not particularly practical for the operator to [d]270x540 to operate on entire columns of entire fields. Therefore, in accordance with the present invention, and in a manner described below, the filter [f]s operates vertically on residual and I blocks as they arrive, see col. 8 line 26-31. Since a macroblock is contains four luminance pixels and Fimoff discloses that it is not practical for the operator to operate on entire columns of entire fields, and to operates vertically on residual and I blocks as they arrive, it is clear to the examiner that Fimoff more than fairly suggest and teaches to operate on the luminance pixels of a block as they arrive, which reads upon the claimed limitation.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the image block contains luma portions, since it is well known that a macroblock contains 4 luminance blocks.

Regarding claim 12, Fimoff (modified by Yuan and AAPA) as a whole teaches everything as claimed above, see claim 11. In addition, Fimoff teaches the video decoder of claim 11, wherein: during a second cycle: the register receives pixels of a macroblock; and the pixel reconstructor applies offsets to said reference pixels for the macroblock, thereby resulting in the macroblock (However, Fimoff teaches a method of reconstructing pixel blocks from P and B DCT coded blocks comprises the following steps: a) selecting reference pixels from a memory in response to a motion vector; b)filtering the selected reference pixels to produce a filtered output; c) if the motion vector has 1/2 pixel resolution, adding a drift compensation value to the filtered output; and, d) adding the filtered output to the P and B DCT coded blocks in order to form the reconstructed pixel blocks. Thus, it is clear to the examiner that Fimoff teaches where

Fimoff does not explicitly disclose a register the first half of the row of luma portions; and second half of a row of luma portions.

However, Fimoff does disclose a memory (col. 6 line 50-58) and that in a decoder, it is not particularly practical for the operator to [d] 270x540 to operate on entire columns of entire fields. Therefore, in accordance with the present invention, and in a manner described below, the filter [f]s operates vertically on residual and I blocks as they arrive, see col. 8 line 26-31. Since a macroblock contains 4 luminance blocks which are composed of pixels, and Fimoff teaches where it is not practical for the operator to operate on entire columns of entire fields, and to operates vertically on residual and I blocks as they arrive, it is clear to the examiner that Fimoff more than

fairly suggest and teaches to operate on the pixels in a luminance block as the pixels arrive, which reads upon a the claimed limitation.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the image block contains luma portions, since it is well known that a macroblock contains 4 luminance blocks.

7. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al., US- 5,920,353 in view of Applicants Admitted Prior Art (AAPA) in view of Moon US-6, 222,467 and further in view of Ueda et al., US-2002/0009287.

8. Regarding claim 5, Diaz teaches a pixel reconstructor (fig. 3) for decoding macroblocks, said pixel reconstructor comprising: a macroblock input buffer (FIFO, fig. 3); a multiplexer connected to the macroblock input buffer (MUX, fig. 3). Diaz is silent in regards to the macroblock input buffer for storing reference pixels that are referenced by at least one motion vector, a register connected to the multiplexer for storing a portion of the reference pixels that are referenced by the at least one motion vector; and a data path connected in parallel to the register.

However, APPA a register for storing a portion of the reference pixels that are referenced by the at least one motion vector (During decoding, the motion vectors are used to retrieve the reference pixels. The reference pixels are retrieved from a memory storing the reference frame. The memory storing the reference frame is known as a frame buffer. A motion vector address computer determines the appropriate addresses storing the reference pixels for a macroblock, based on motion vectors, [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Fimoff (modified by Yuan) with AAPA for providing efficient image processing.

Diaz (modified by AAPA) is silent in regards to a register connected to multiplexer, and a data path connected in parallel to the register; a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector.

However, Moon discloses multiple registers connected to more than one multiplexer (first-sixth registers, fig. 3 and first – second multiplexers). Further discloses by Moon is that the registers have common pathways between the registers and multiplexers (fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decompression device of Diaz (modified by AAPA) with the teaching of Moons' multiple registers and multiplexers to provide a more efficient decoder that increases the speed of the video decoder, bitstream decoder and the operating clock frequency (Moon, column line 31-47).

Diaz (modified by AAPA and Moon) is silent in regards to a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector.

However, Ueda teaches a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector (When a macroblock output from the decoder 15 needs motion compensation, the motion compensation circuit 16 reads the reference pixel data from the video buffer in the buffer via the buffer control circuit 123 in accordance with the prediction vector output from the decoder 15. The obtained reference pixel data is added to pixel data supplied by from the decoder 15 thereby

performing motion compensation [0058]. Since Ueda discloses reference the pixels are read from the video buffer, and are supplied to the decoder thereby performing motion compensation, and motion compensation produces a motion vector, therefore, it is clear to the examiner that Ueda teaches to a macroblock buffer that stores reference pixels that are referenced by at least one motion vector.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Ueda with Diaz (modified by Moon) for more efficient image processing.

Regarding claim 6, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teaches a macroblock input buffer register connected to the multiplexer (Moon, first register; fig. 3). Further Moon discloses registers first through second connected to the second multiplexer.

Regarding claim 7, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teaches another multiplexer connected to the register ((Moon, second register; fig. 3). Further Moon discloses registers first through second connected to the second multiplexer.

Regarding claim 8, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teaches a bypass path connected to the macroblock input buffer and the another multiplexer, said bypass path bypassing the multiplexer and the multiplexer input buffer register (Moon discloses where the data from the second register can either be received by either the first or second multiplexer from the variable length decoder, fig. 3).

Regarding claim 9, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teach to reconstruct pixels from macroblocks encoded in accordance to a plurality of standards (Moon discloses MPEG-1, MPEG-2, H.261, and H.263; column 6 line 5-7).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al., US- 5,920,353 in view of Applicants Admitted Prior Art (AAPA) in view of Moon US-6, 222,467 in view of Ueda et al., US-2002/0009287 and in further view of Yuan et al., US-2005/0094729.

10. Regarding claim 10, Diaz (modified by AAPA, Moon and Ueda) as a whole are silent in regards to wherein the plurality of standards comprises MPEG-2 and AVC. However, Yuan teaches this limitation (Yuan, fig. 4, 6, and 8). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Yuan with Diaz (modified by AAPA, Moon, and Ueda) to include the standard of AVC for maximizing flexibility and adaptability of the system, thus allowing for support for video and audio application of different standards and formats without significant hardware overhead (Yuan, [0037]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSICA ROBERTS whose telephone number is (571)270-1821. The examiner can normally be reached on 7:30-5:00 EST Monday-Friday, Alt Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner, Art Unit 2621